Code :R7321504 1

III B.Tech II Semester(R07) Regular & Supplementary Examinations, April/May 2011
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Systems Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE questions
All questions carry equal marks

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1. Explain about the following:
   (a) Semiconductor DRAM.
   (b) Principle of locality.
2. How do you classify Instruction set Architectures?
3. Explain about Tomasulo's Algorithm in detail.
4. (a) Explain about Software Pipelining.
   (b) Explain about Global Code Scheduling.
5. Define miss rate. Briefly explain the miss rate reduction techniques.
6. (a) Explain cache coherence protocols.
   (b) Explain cache coherence state chart diagram.
7. What is RAID? Explain different levels of RAID.
8. Explain interconnection network media.

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Code :R7321504 2

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Time: 3 hours Max Marks: 80

Answer any FIVE questions
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1. Explain CPU performance equation in detail.
2. Explain the types of Instruction set architectures.
3. Describe various techniques for overcoming Data hazards.
4. Discuss about Compiler Speculation with Hardware Support.
5. (a) Explain "compiler optimizations".
   (b) Explain the divisions of conflict misses and how they are calculated.
6. (a) Explain how locks are implemented using coherence?
   (b) Discuss "write invalidate protocol".
7. Explain about magnetic disks and optical disks.
8. (a) Describe cross company interoperability.
   (b) Explain about designing a cluster with an example.

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Code :R7321504 **3**

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(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks

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1. Explain with an example the distribution of cost in a system.
2. Explain different types of addressing modes in detail.
3. Explain about different types of dependencies in detail.
4. Write about the Itanium Processor in detail.
5. (a) Briefly describe the typical memory hierarchy.
   (b) Explain strategies for how a block found if it's in main memory.
6. (a) Explain the synchronization and its hard ware primitives.
   (b) Explain the example for directory based protocols.
7. (a) Explain about transaction bench marks.
   (b) Draw neat sketch for split transaction bus. Explain.
8. (a) Explain generic inter connection network.
   (b) Explain the bridges, routers and SAN.

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Code :R7321504 4

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Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks

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1. Discuss about Technology trends in detail.
2. Compare different types of addressing modes.
3. Explain about Dynamic Scheduling using Tomasulo's approach.
4. Write about the Transmeta Crusoe Processor in detail.
5. Explain the protection mechanism for virtual memory.
6. (a) What are states of directory based cache coherence protocols? Explain.
   (b) Draw the state transition diagram for the directory has the same states and structure for an individual cache. Explain.
7. Explain the steps in designing an I/O system.
8. Explain about fiber optics, twisted pair and coaxial cable.

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